Proceedings of the XVI International Conference on Thermoelectrics, Dresden, Germany, p. 641, 1997

Thermoelectric Microcoolers for Thermal Management Applications

J.-P. Fleurial, A. Borshchevsky, M.A. Ryan, W. Phillips, E. Kolawa, T. Kacisch and R. Ewell
Jet Propulsion Laboratory/California Institute of Technology, Pasadena, California, USA

Abstract

Due to the combined increase in circuit integration and chip power dissipation, there is a rapidly growing demand for solving the thermal management issues of power microelectronics. We are pursuing a novel thermal management approach that actively cools only the key high power devices by using a novel thermoelectric microcooler located under each of these power devices. In this way the device can operate at temperatures at or even below the ambient temperature of the heat sink, resulting in increased reliability and efficiency. To successfully handle the high heat flux densities generated at the back of the power chips, a microcooler with thin legs and low thermal resistance at the interfaces must be built. We are currently developing a thermoelectric microcooler combining thick films of Bi_2Te_3-based alloys and very high thermal conductivity substrates, such as CVD diamond or AlN.

Electrochemical deposition is a very attractive process for depositing thick films of compound semiconductors on metallic surfaces. This paper presents recent results on the deposition of Bi_2Te_3 and related ternary solid solutions on a variety of metallic substrates. We also report on the development of Cu diffusion barriers for Bi_2Te_3 and stable metallizations and diffusion barriers for diamond and AlN substrates.

Introduction

The demand for increased processing speeds of integrated circuits, computers and other electronic systems requires higher power levels and a higher packaging density. The designing of microprocessors with faster clock rates call for faster logic, which necessitates more power, while an increase in the functional density of processors also results in a larger power requirement. In addition the growing digitalization and miniaturization of portable civilian and military electronic equipment necessitates ever increasing levels of integration between electronics, power sources and thermal control. Combined, these requirements result in very high power densities and thermal problems, which limits integration of devices and components.

At the chip level, the highest performance can be obtained if the junction temperature can be maintained at a tolerable level. Ideally, a reduced temperature and a closely controlled thermal environment is needed. Already, many high power electronic devices, such as power amplifiers and microprocessors, operate at high temperatures close to or at the edge of their reliability, which can severely impact performance and operating lifetime. Next generation power electronic chips, such as solid state power amplifiers, used for microwave applications, will have much higher power levels, with thermal power dissipation requirements increasing from 5 W to 30 W within a few years [1]. That increase will multiply the heat flux that has to be removed, from approximately 30 W/cm^2 to several hundreds W/cm^2. This higher heat flux density will result in a major thermal management problem that will have to be addressed using novel techniques. This is illustrated in Figure 1, which shows preliminary results from a thermal model of a next generation 20W GaN-based power amplifier with a 1.5x1.5 mm^2 footprint of which only 250x250 μm^2 is constituted by the electronic active layer. The very high heat flux densities in the immediate vicinity of the active layers (over 16000 W/cm^2) lead to an estimated 75-110°C temperature difference with respect to the back of the SiC substrate which still presents heat flux densities on the order of 100 W/cm^2.

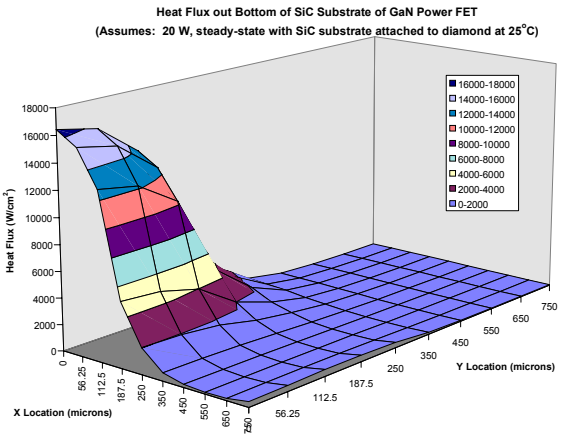

Figure 1: Heat flux profile for a 20W GaN FET using a 5 μm GaN buffer layer on top of a self-standing 100 μm SiC substrate, assuming steady state operation.

Conventional thermal management techniques are not well suited to the specific problem of cooling discrete or localized heat dissipating devices since they generally cool the whole board. Moreover these techniques have difficulty dealing with the large heat fluxes associated with the high density packaging of power devices. The specific problem of spot cooling of power devices can be very effectively solved by using a combination of diamond substrates and a thermoelectric microcooler. The highest power components would be mounted directly on a diamond substrate (ideally the top substrate of the cooler) allowing the cooler/diamond combination to maintain the temperature of the device from a few degrees to tens of degrees below that of the substrate on which the cooler is mounted (diamond or any other high thermal conductivity material such as AlN) and thermally connected to the heat sink. The cold side diamond substrate will allow "thermal lensing" or spreading of the heat load as uniformly as possible onto a larger surface (for example such

as a 10x10 mm^2 surface from the initial 1.5x1.5 mm^2 chip footprint). This will reduce the heat flux density to be cooled by the thermoelectric device from thousands of W/cm^2 to a more manageable 100-150 W/cm^2. The thermoelectric microcooler will then offset part of the temperature gradient across the chip substrate and allow the device to continuously operate at a low enough temperature to increase both reliability and clockspeed.

The main disadvantage of using thermoelectric coolers is the rejection of additional heat due to their low coefficients of performance (COP) at large temperature gradients. This additional heat has to be removed from the heat sink so an additional cooling technique is needed, such as a high thermal conductivity substrate, a heat pipe, microchannels or spray cooling [2-4]. The COP obviously varies over a large range depending on the temperature difference required, the thermal conductivity of the substrates and the thermal gradient. The cooling power density of state-of-the-art (SOA) bulk coolers is limited, which is why it is necessary to increase miniaturization in the cases of large heat fluxes.

Thick Film Microcoolers

The main benefit of going to thick film coolers is the dramatic increase in cooling power density which is inversely proportional to the length of the thermoelectric legs. Preliminary estimates have shown that heat flux densities up to several hundred W/cm^2 can now be removed with thick film coolers, with cooler leg lengths on the order of 10 to 50 μm.

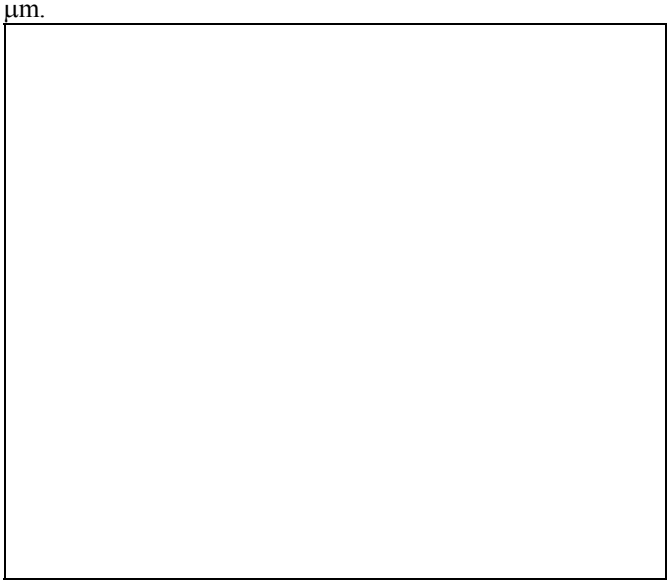

Fig. 2: Cooling power densities as a function of the temperature gradient across the thermoelectric device for three different kinds of coolers.

Figure 2 shows the cooling power density comparisons for a SOA commercial cooler with 2mm legs, for a bulk micro-cooler with 200μm legs, and for a thick film cooler with 20μm legs. These curves are for a hot side temperature of 330K and maximum cooling power operation. As can be seen from the figure, the cooling power density of the diamond substrates/thick film cooler combination is approximately two orders of magnitude greater than that for the SOA current cooler and one order of magnitude greater than that for the bulk micro-cooler. The reason to go to thick film coolers is thus very obvious.

Device considerations

However, considerable development work is still needed before thick film coolers are ready to be used. The limiting factors for microcoolers are the magnitudes of the electrical and thermal contact resistances. The contribution of these resistances become important parameters as the thermoelement length becomes smaller. They degrade the performance of the thermoelectric microcooler by decreasing the maximum COP, the maximum cooling capacity and the maximum temperature difference that can be achieved.

For resolving the thermal issues, the use of substrates such as AlN or diamond (thermal conductivity respectively one and two orders of magnitude higher than alumina, see Table 1) is necessary so that as small a ΔT as possible is dropped across the substrate. Assuming a uniform heat load on the cold side substrate, the performance of alumina based coolers was calculated and plotted in Figure 2. For the 20 μm cooler, the temperature gradient "lost" across alumina substrates ranges from 12 to 25°C, depending on the heat load. Moreover, if one considers a real case power chip with a much smaller footprint than the top cooler substrate, even larger additional temperature gradients will appear in the plane of the substrate (poor heat spreading). This will result in unacceptable operating temperatures for the power device being "cooled" (in some cases temperatures might even be higher with the alumina based cooler than without it).

For miniaturized thermoelectric devices comprised of thousands of thermoelements, electrical contact resistances can become a very large fraction of the total internal resistance. The degradation in performance for high electrical contact resistance values is illustrated in Figure 3. Low contact resistances (close to $1x10^{-6}$ $\Omega.cm^2$) can relatively easily be obtained using thin film processing technology developed for electronic semiconductors [5].

Table 1: Electrical resistivity (ρ in 10^{-8} Ω.cm), thermal conductivity (λ in W/mK) and thermal expansion coefficient (α in 10^{-6} K) at 300K of elements and compounds for thermoelectric microcoolers.

	Diamond	AlN	Al_2O_3	Ni	Pt	Cu	Bi_2Te_3
ρ				6.84	9.85	1.68	1000
λ	~1800	~180	20	91	72	400	1
α	1.5	4.4	7.1	13.3	9.1	16.4	12.9

In addition to the thermal and electrical contact resistances, other issues such as heat losses, mechanical strength and stress analysis must be considered. The low thermal expansion coefficient of diamond is of particular concern (see Table 1) to the ruggedness of thermoelectric microdevices, and where appropriate from a thermal and cost aspect, AlN offer a better match to Cu and Bi_2Te_3.

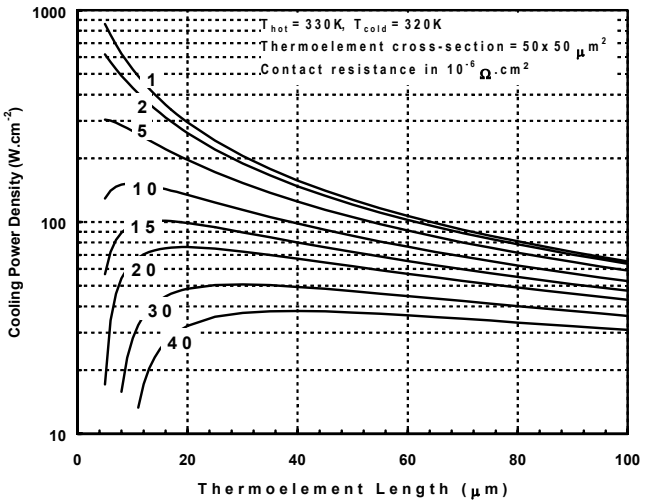

Figure. 3: Cooling power densities as a function of the thermoelement length and for increasing electrical contact resistances at the thermoelement/Cu electrode interface. Calculations performed for diamond-based microcoolers operating across a temperature gradient of 10°C.

Microcooler fabrication

Areas under development at JPL are the deposition and characterization of Bi_2Te_3-based thick films, bonding of metallized diamond or AlN substrates to the thermoelectric films, and the patterning, etching, bonding and testing of the cooler. Figure 4 shows the proposed schematic for the metallizations and bonding scheme for the diamond and the thick film thermoelectric material.

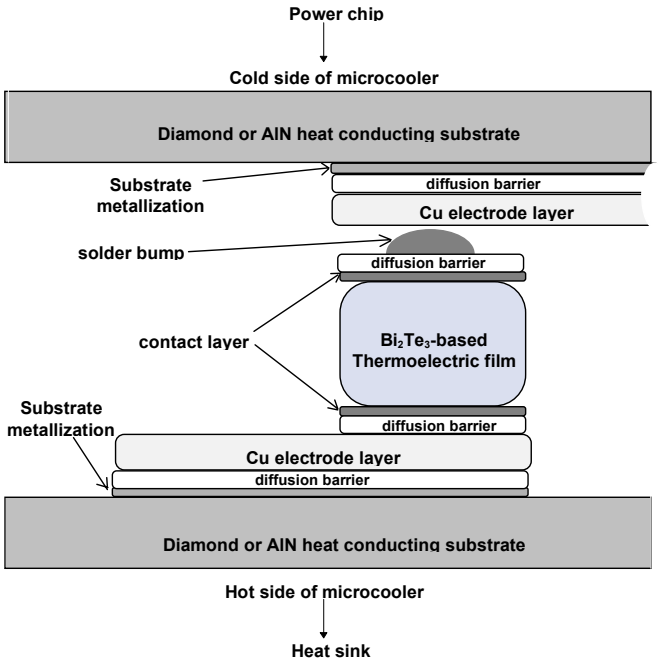

Figure 4: Schematic of a thick film thermoelectric cooling device with diamond or AlN substrates.

The scheme, similar to that for traditional bulk thermoelectric modules, involves many layers, including metallization to the high thermal conductivity substrate, diffusion barrier, Cu electrode, Cu diffusion barrier, contact layer and Bi_2Te_3 alloy film. Except for the Cu electrode and the thick thermoelectric film, all other metallic layers are of submicron thickness.

Thermoelectric Thick Films

A promising route for thick film preparation is electrochemical deposition (ECD) from aqueous solution. This is a fairly well known technique for the deposition of II-VI semiconductors such as CdSe, CdTe $CdSe_{0.5}Te_{0.5}$ and $CdSe_{0.65}Te_{0.35}$ [6,7]. In this technique the elements are deposited on an electrode using an aqueous solution of anions or anionic compounds. The advantage of this approach to the fabrication of films is that it is an inexpensive way to make films and, depending on the current density used in deposition, the deposition rate can be varied widely. Thick films can be difficult and time consuming to make using vacuum techniques such as sputtering or evaporation, but films several tens of microns thick can be made in a few hours using electrochemical deposition. In addition, slight variations in the deposition potential or solution concentration may possibly be used to induce off-stoichiometric films, thus providing p- or n-type doping through stoichiometric deviation. The preparation of thermoelectric material films by electrodeposition has been investigated very little [8,9] and the methods used in making the II-VI alloys must be adapted to the electrodeposition of thin films with p-type and n-type $Bi_{2-x}Sb_xTe_{3-y}Se_y$, compositions which are optimal for thermoelectric cooling applications. An additional advantage of this approach to the fabrication of thin film thermoelectric coolers is that some of the contact layers necessary to the fabrication of the cooling device, such as Cu for the electrical path or Ni or Pt for the Cu diffusion barrier can also be deposited by using a different aqueous solution.

Bismuth and tellurium metals dissolve in HNO_3 to make the oxide anions BiO^+ and $HTeO_2^+$. Bi_2Te_3 is insoluble in dilute HNO_3, so reduction of $HTeO_2^+$ to Te^{2-} at an electrode will result in the precipitation of Bi_2Te_3 on the electrode surface. The overall reaction for the process is:

$$13H^+ + 18e^- + 2BiO^+ + 3HTeO_2^+ \rightarrow Bi_2Te_3\downarrow + 8H_2O$$

Figure 5 shows the current-voltage behavior of an aqueous solution of $7x10^{-3}$ M BiO^+ and $1.0x10^{-2}$ M $HTeO_2^+$ in 1 M HNO_3. The reduction regions for each of these compounds overlie each other in the range -0.05 to -0.2 V versus a standard calomel electrode. BiO^+ is reduced to Bi^0 around -0.1 V. It is possible to co-deposit Bi_2Te_3 within this voltage range, probably more effectively in the range 0 to -0.1 V than within the region of the reduction wave for BiO^+. Preliminary studies have shown that variation in grain size and composition of the films can be introduced by changing the potential at which the deposition is carried out toward 0 V, as well as by changing the concentration of ions in solution.

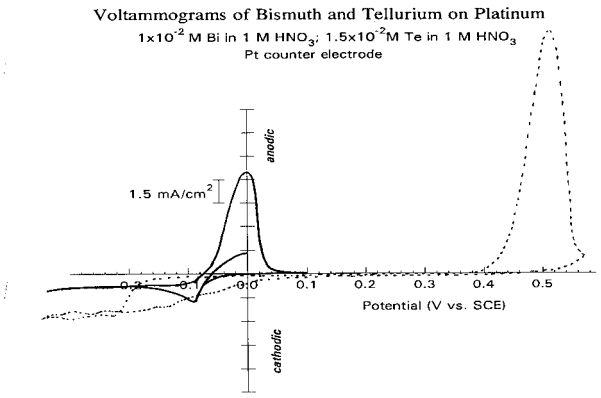

Figure 5: Current-Voltage graph for the electrochemical deposition of Bi and Te on a Pt substrate using a nitrate aqueous solution. (SCE is for standard calomel electrode)

Other parameters controlling the quality, composition and properties of the Bi_2Te_3 films grown by ECD are: temperature, Bi and Te molar concentrations in the HNO_3 solution, deposition time, substrate surface finish and geometry, active stirring of the bath, volume of the bath, distance between counter and deposition electrodes, and characteristics of the reference electrode. Such a large number of parameters means that many experiments (several thousand) must be run to determine the best experimental parameter values. We are currently developing a combination of statistical tools based on orthogonal arrays of control parameter values to optimize this deposition process and determine in a small number of experiments the best conditions for depositing high quality Bi_2Te_3-based films with good thermoelectric properties.

Initial deposition runs on Pt-coated substrates have shown that thick near-stoichiometric Bi_2Te_3 films could be grown from a $0.75x10^{-2}$ M/l [Bi] and $1.0x10^{-2}$ M/l [Te] concentrations. The thickness of the films measured with a profilometer ranged from 10 to 60 μm and the composition of the films was very close to the 40/60 at% ratio, as determined from electron microprobe analysis. In addition, back-scattering electron analysis indicated that films grown at low deposition voltages had very smooth top surfaces (less than 1 μm of roughness). The growth rates ranged from 10 to 20 μm/hour depending on the deposition voltage.

Measurements of the electrical transport properties has been conducted on some of the deposited films. Van der Pauw electrical resistivity and Hall effect were measured in the plane of the deposited films (after removal from the metallized substrates), and the Seebeck coefficient was measured in a cross-plane direction. Our results show heavily doped n-type behavior and are similar to those obtained previously by [9] except that we have achieved lower electron concentrations (~ $1x10^{20}$ cm^{-3}) and higher Hall mobility values (~ 26 cm^2/Vs). Seebeck coefficient values range from -50 μV/K to over -100 μV/K near room temperature. We are now working on optimizing the properties for n-type films as well as studying the possibility of achieving p-type conductivity. Recent experiments on ternary compositions demonstrated that $Bi_2Te_{3-x}Se_x$ ($0<x<0.1$) and $Bi_{2-y}Sb_yTe_3$ ($1.5<y<2$) films could also be obtained by ECD. Detailed experimental results will be published later [10].

Cu Diffusion Barrier

For the multilayer stack, Cu will be used for the electrical path (electrode) of the thermoelectric device, because Cu has low electrical resistivity and high thermal conductivity values (see Table 1), and can easily be deposited electrochemically. However a diffusion barrier must be found to prevent Cu from diffusing into Bi_2Te_3 and degrading the thermoelectric properties. Ni is the Cu diffusion barrier of choice in the thermoelectric industry, but unfortunately we have found that the Ni layer is dissolved in the nitrate solution used to grow Bi_2Te_3 by electrochemical deposition. After considering several options including a protective layer over the Ni barrier, the possibility of more suitable diffusion barriers was investigated.

Potential candidates included Cr, Pd and Pt as well as highly thermally stable amorphous nitride films previously developed for metallizations to diamond and AlN [5]. However, studies were required to demonstrate their effectiveness as diffusion barriers for Cu and to demonstrate that they do not contaminate the Bi_2Te_3 film.

A number of experiments were conducted on single crystalline Bi_2Te_3 bulk samples which were coated with Pt/Cu, Pd/Cu, Ni/Cu, Cr/Cu, TiSiN/Cu and TaSiN/Cu. The diffusion barrier thickness was typically 150 nm and the Cu overlayer was 250 nm. Several samples were prepared for each multilayer combination, and some of the samples were annealed for 1 hour at 150°C, 200°C, 250°C or 350°C in high vacuum. After completion of the anneals, as-coated and annealed samples for each materials combination were analyzed by Rutherford backscattering (RBS) microscopy.

Results showed that for temperatures in the 150-250°C range only Pt and the amorphous nitrides are suitable diffusion barriers (no Bi or Te detected on top of the Cu). For temperatures higher than 250°C the nitride films performed best. Both Ni and Cr samples showed some interdiffusion even at 150°C, and catastrophic results were obtained with Pd. Detailed results will be reported elsewhere [11]. Despite the apparent negative result of Ni as a Cu diffusion barrier, it must be noted that thermoelectric coolers are typically soldered at only 138°C (some at 189°C), and operated at 50-75°C maximum (hot side). Since Pt is well suited to the electrochemical deposition of Bi_2Te_3, we are now developing a Cu electrode/Pt barrier/Bi_2Te_3 combination by ECD.

Conclusion

The demand for increased speeds and higher power levels for electronic devices such as power amplifiers and microprocessors has resulted in thermal problems on the component and board level that need to be solved. The spot cooling of these power devices and microprocessors is needed to increase reliability, efficiency, and clockspeed. Thermoelectric microcoolers using high thermal conductivity substrates such as diamond or AlN are one of the most promising methods to address these thermal management issues. Very high cooling power densities (over 100 W/cm^2) can be achieved with thick film coolers. We are currently developing such devices using a promising electrochemical technique to deposit Bi_2Te_3-based film on metallized and patterned diamond substrates.

Acknowledgments

The work described in this paper was performed at the Jet Propulsion Laboratory/California Institute of Technology under contract with the National Aeronautics and Space Administration. Part of this work was supported by the Ballistic Missile Defense Organization and managed by Wright Laboratory, WL/POO, MIPR # NFY14559600672.

References

1. P. Smith, Jet Propulsion Laboratory, private communication.
2. M.T. North, D.B. Sarraf, J.H. Rosenfeld, Y.F. Maidanik and S. Vershinin, *Proc. Space Technology and Applications International Forum*, AIP 387, 2, 561-566 (1997).
3. M.M. Sherman and G.O. Campbell, *Proc. Spacecraft Thermal Control Symposium*, Albuquerque, Nov. 1994
4. Isothermal Systems Research Inc., private communication.
5. E. Kolawa, J.S. Chen, J.S. Reid, P.J. Pokela, and M-A. Nicolet, *J. Appl. Phys.* 70, 1369 (1991).
6. K. Rajeshwar, *Adv. Mater*., 4, 23 (1992) and references therein.
7. Y. Mirovsky, R. Tenne, G. Hodes and D. Cahen, *Thin Solid Films*, **91**, 49 (1982).
8. M. Takahashi, Y. Katou, K. Nagata and S. Furuta, *Thin Solid Films*, 240(1-2), 70 (1994).
9. P. Magri, C. Boulanger and J.M. Lecuire, *J. Mater. Chem*., 6 (5) 773-779 (1996).
10. M.A. Ryan, A. Borshchevsky, W. Phillips, J.-P. Fleurial and T. Caillat, to be published in the Journal of the Electrochemical Society.
11. T. Kacisch, E. Kolawa, J.-P. Fleurial, T. Caillat and A. Borshchevsky, to be published.