Thermoelectric Microdevice Fabrication Process and Evaluation at the Jet Propulsion Laboratory (JPL)

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Abstract

Advances in the microelectronics industry have made it possible to fabricate a multitude of microdevices, such as microprocessors, microsensors, microcontrollers, and microinstruments. These electronic microdevices have significantly reduced power requirements but at the same time require more attention in terms of integrated thermal management and power management and distribution. Micro thermoelectric converters are considered a promising technology approach for meeting some of these new requirements.

Thermoelectric microdevices can convert rejected or waste heat into usable electric power, at moderate (200-500K) temperatures and often with small temperature differentials. They can also be easily integrated and provide effective cooling for devices specific in optoelectronics, such as mid-IR lasers, dense-wavelength-division-multiplexing (DWDM) components and charge-coupled-device (CCD) detectors.

In the Materials and Device Technology Group at JPL, we have developed a unique fabrication method for a thermoelectric microdevice that utilizes standard integrated circuit techniques in combination with electrochemical deposition of compound semiconductors ($Bi_2Te_3/Bi_{2-x}Sb_xTe_3$). Our fabrication process is innovative in the sense that we are able to electrochemically micro mold different thermoelectric elements, with the flexibility of adjusting geometry, materials composition or batch scalability. Successive layers of photoresist were patterned and electrochemically filled with compound semiconductor materials or metal interconnects (Au or Ni). A thermoelectric microdevice was built on either glass or an oxidized silicon substrate containing 63 couples (63 n-legs/63 p-legs) at approximately 20 microns in structure height and with a device area close to 1700 μm x 1700 μm. In cooling mode, we evaluated device performance using an IR camera and differential thermal imaging software. We were able to detect a maximum cooling effect of about 2K. In power generation mode, a 75 watt light source was illuminated directly above the device while the current generated was measured. A detailed step-by-step overview of the fabrication process will be given, as well as specifics in testing setups, results and future directions.

Introduction

As a spacecraft travels further away from the sun, for a defined solar panel surface area, solar flux decreases accordingly (inverse square law) and loses effective power. Spacecraft that travel beyond the orbit of Mars or that require longer lasting power systems require a source of electric power other than solar energy. For missions such as Cassini (launched 1997 to study the Saturn system), radioisotope thermoelectric generators (RTGs) are used for power [1]. Thermoelectric devices take advantage of the Seebeck effect for power generation and can also utilize the Peltier effect for active cooling. Thermoelectric coolers have various applications for microprocessors, medical analyzers, portable picnic coolers and many more. In the optoelectronics industry, thermal management is a significant factor in optimizing device performance. For instance, due to excessive heat generated, there are compromises in laser wavelength stability and increased noise levels in detectors [2].

In the past few years, advancements in the microelectronics industry have made it possible to miniaturize components, devices, instruments and even spacecraft. With the miniaturization of electronic devices, there has also been a concomitant focus on developing miniaturized power conversion and thermal management systems. Miniaturizing thermoelectric converters will enable milliwatt power at several volts for MEMS devices and other microinstruments [1,3]. Additionally, thermoelectric micro coolers offer effective and practical options for precise thermal management in compact optoelectronic devices. A few applications include spot cooling for mid-IR lasers and CCD detectors [4].

An encouraging approach for meeting various power requirements, while simultaneously being able to offer adequate thermal control, are micro thermoelectric converters. These thermoelectric microdevices can operate at moderate (200-500K) temperatures and with small temperature differentials. For the temperature range of 200-500K, alloys based on n-type Bi_2Te_3 and p-type $Bi_{2-x}Sb_xTe_3$, are the best materials suitable for numerous optoelectronic and micro spacecraft applications [1].

According to scaling laws [1,3], the attractive idea behind a thermoelectric microdevice is to increase specific power (W/cm^2) by reducing the size of the thermoelectric elements, while maintaining the same aspect ratio of elements in a larger thermoelectric device. Equally important, miniaturization increases maximum cooling and improves cooling densities [5]. A thermoelectric module generally consists of several n- and p-type leg elements (couples) connected in series electrically and in parallel thermally. A microdevice will enable potentially thousands of these couples to be connected together in a very small area, leading to open circuit voltages of several volts at even modest temperature gradients [1,3].

At the Jet Propulsion Laboratory (JPL), we have fabricated thermoelectric microdevices using a combination of integrated circuit processing techniques and electrochemical deposition

of compound semiconductors (Bi_2Te_3/ $Bi_{2-x}Sb_xTe_3$) [6-8]. It was possible to construct micro power generators/coolers with leg elements approximately 20 microns tall and approximately 60 microns in diameter (varies somewhat due to conical shape of legs). A thermoelectric microdevice was built on either glass or an oxidized silicon substrate(Si/SiO_2) containing 63 couples (63 n-legs/63 p-legs) and with a device area close to 1700 μm x 1700 μm. Microdevices were tested and evaluated for power generation and effective cooling performance.

Electrochemistry and Materials Properties

Electrochemical deposition (ECD) offers an inexpensive and scalable process [9]. Materials can be varied in composition with deposition rates up to several tens of microns per hour.

N-type Bi_2Te_3 and p-type $Bi_{2-x}Sb_xTe_3$ compounds were deposited at room temperature at constant potential (EG&G PAR 273A) in a standard three electrode configuration. The working electrode was either a metallized glass or metallized oxidized silicon substrate. The cell had a Pt counter electrode and a saturated calomel electrode (SCE) reference. Regions for deposition were defined using a patterned photoresist mask.

Thermoelectric leg elements were deposited from solutions containing dissolved elemental metals with a concentration on the order of 10^{-3} M in aqueous 1 M HNO_3 (pH=0). Solutions containing Sb use chelating agents such as citrate, tartrate or ethylene diamine tetraacetate (EDTA) to allow higher concentrations of the less soluble element at pH 0 [1,3].

Leg elements have been electrochemically formed, however with different thermoelectric properties from that of bulk materials. Due to difficulties in obtaining material properties from individual leg elements, we instead measured ECD films (1 cm^2, ~10 μm thick). As deposited Bi_2Te_3 films exhibited heavily doped n-type behavior with dense growth. EDX analysis confirmed near Bi_2Te_3 stoichiometry. Bi_2Te_3 material properties are as follows: Seebeck = -30 to -60 μV/K, ρ ~ 1 mΩcm (in plane), n ~ 1 x 10^{20} cm^{-3} and μ_H ~ 15-25 $cm^2V^{-1}s^{-1}$.

ECD p-$Bi_{2-x}Sb_xTe_3$ properties have not been fully characterized because of inconsistencies in reproducibility. Material compositions were found to be very sensitive to initial electrolyte concentrations and deposition voltages. At Sb-rich or near Sb_2Te_3 stoichiometry, desirable dense morphologies were attained but at the sacrifice of Seebeck values. Upon increasing Bi content, both film and leg elements resulted in unfavorable dendritic/columnar growth. Leg morphology is critical to device fabrication and performance. It is extremely difficult to fabricate complete devices if the tops of the electrodeposited legs are too rough (mentioned later). Also, these low density or porous ECD materials are characterized by higher resistivities and reduced mechanical integrity. Leg elements with low mechanical strength are susceptible to stress induced horizontal cracking, which dramatically increases resistivity or ultimately leads to device failure. Nonetheless, even with incomplete materials characterization, preliminary observations indicate that annealing ECD materials at 250°C have promising effects [10].

Commercially available gold and nickel bath solutions were used for ECD of bottom base dogbone contacts and top interconnects.

Photolithography

Photolithographic patterning was performed with a Solitec 3000 HR mask alignment and exposure system (UV power at 750 watts). Two different positive photoresists, Microposit SJR 5740 (Shipley) and Clariant AZ 1518, were used with corresponding Microposit 453 developer and AZ developer. Photoresists were spin coated with a Headway Research, Inc. Photo-Resist Spinner Model 1-PM101DT-R790 and baked on a Cole Parmer 04644 Series Digital Hot plate. Laser printed transparency film and glass masks were designed using Autodesk AutoCAD 2000 Architectural Desktop and printed by CCI Graphics.

Successive layers of photoresist were applied as scaffolding for the micro molding of connected thermoelectric couples.

Fabrication Process

A. Substrate Preparation

Device fabrication begins with substrate selection of either a glass (Corning 2947 MicroSlides 75 x 50 mm, 1 mm thick) or an oxidized silicon (Si/SiO_2, 37.5 mm x 50 mm, 0.381 mm thick) substrate. After substrate cleaning and drying, a Cr adhesion/conduction layer (few hundreds of Å) followed by a Au electrode layer (~2000 Å), are Argon plasma deposited using a large custom built RF sputtering system. The Au/Cr substrate is then cut in half with a diamond scribe to two 37.5 mm x 50 mm samples, if not already cut to size (silicon substrates). Substrates at this size can accommodate eight microdevices.

B. Domino 8 Dots

Next, AZ 1518 photoresist is spin coated on the gold side of the substrate and baked on a hotplate. A transparency mask with the Domino 8 Dots pattern (Figure 1a) is placed on the sample to expose eight, 0.5 cm diameter dots. Afterward, approximately 2 to 3 micron thick gold is electrochemically deposited within the eight dots to later serve as the bottom base contacts of each couple. The photoresist is then removed with acetone (Figure 1b).

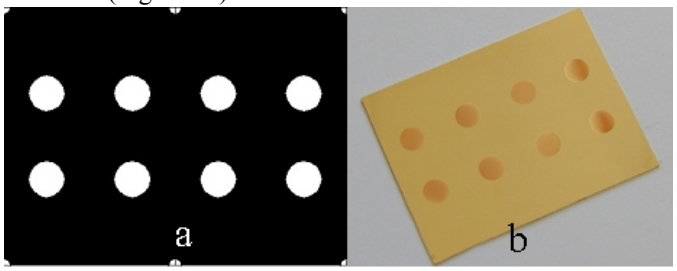

Figure 1. a) Domino 8 Dots mask. b) Gold 0.5 cm diameter dots after ECD on Si/SiO_2 substrate.

C. Flower/Dogbone patterns

Another thin layer of AZ 1518 photoresist is spin coated and baked. A different transparency mask, containing the flower petal contact leads, dogbone base electrodes and crosshair alignment mark patterns (Figure 2a), is placed over

the sample. Each device pattern is aligned over a gold dot to expose outlined device patterns. After completing a gold etch, remaining photoresist is again removed (Figure 2b,c) Devices were designed so that individual or multiple strings (series of 10 or 11 couples) can be addressed, thereby avoiding total device failure from one nonworking string. Illustrated in Figure 2a and more closely in Figure 6b, making contacts to two of the seven petal leads enables individual string or even entire device access (all 6 strings connected in series).

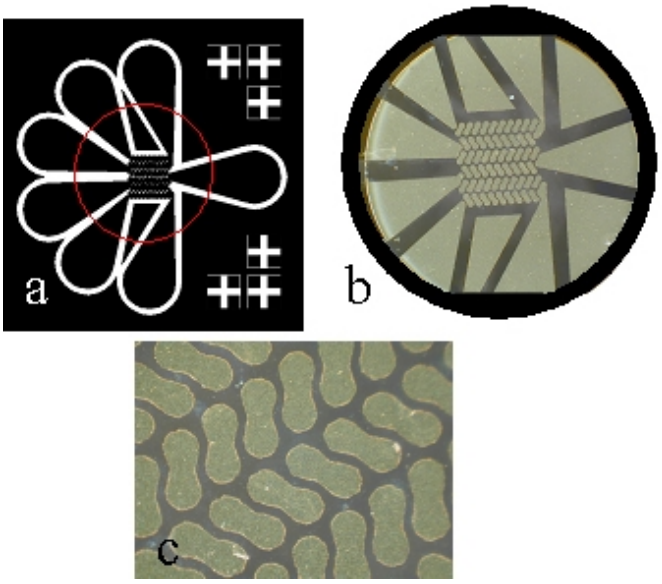

Figure 2. a) Flower/Dogbone mask cutout of one device (8 total on a mask). Circle around the device pattern is not apart of the mask and only indicates ECD gold dot area. b) ECD gold dot area after gold etch. c) Zoom of bottom gold dogbones (each ~270 μm in length).

D. 1st hole opening for p-type leg elements

A thick layer (20 microns) of photoresist (SJR 5740) is spin coated, allowed to rest and then baked. Now, the sample is ready for 1st hole openings on top of one side of each dogbone base electrode. A glass mask with 60 micron diameter holes is used to pattern the 1st holes on one side of each gold dogbone. After photoresist development and roughening of the Au surface, the sample is rinsed, then dipped in the electrochemical bath solution and after ensuring no air bubble clogs the holes, p-type $Bi_{2-x}Sb_xTe_3$ leg elements are grown at constant potential.

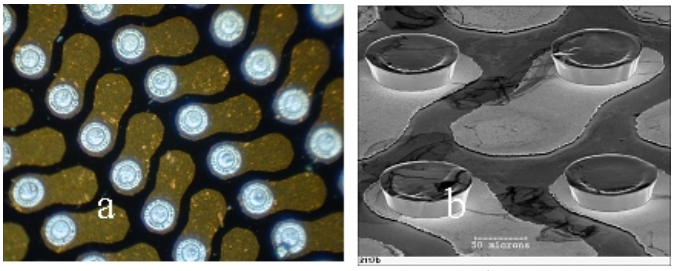

Figure 3. a) ECD p-$Bi_{2-x}Sb_xTe_3$ in 1st hole patterned photoresist. b) SEM of ECD p-$Bi_{2-x}Sb_xTe_3$ leg elements.

E. 2nd hole opening for n-type elements

After ECD of the p-type material (Figure 3a,b) and deposition of a thin photoresist cover layer, a similar mask pattern on the same glass mask, with 60 micron diameter holes, is used to pattern the 2nd holes on the other side of each dogbone (sample rotated 180°). Identical processing steps are copied from the formation of p-leg elements, for the ECD of n-Bi_2Te_3 leg elements (Figure 4).

Figure 4. SEM of ECD p-$Bi_{2-x}Sb_xTe_3$ and n-Bi_2Te_3 leg elements.

After n-leg growth, a flood exposure (no mask) removes the cover AZ 1518 photoresist layer and a very thin layer of gold is sputtered over the entire sample (Edwards Sputter Coater S150B). Proper top nickel interconnect growth depends on this gold layer. Next, a soft layer of photoresist (SJR 5740) is spin coated and baked.

F. Top Nickel Interconnects

At this point, the sample is cut into individual pieces(devices) for easier handling. A glass mask with top dogbone interconnect patterns is placed over corresponding n-/p-legs, aligned and exposed as seen in figure 5.

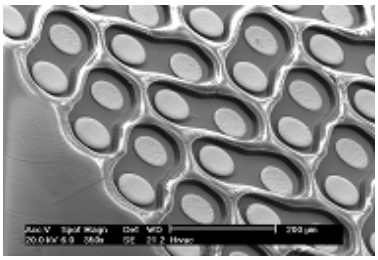

Figure 5. SEM of developed top nickel interconnect patterns

The top nickel interconnects are typically between 2 to 3 microns thick. After ECD of nickel, each top interconnect must be disconnected from each other by removing the thin gold layer, as well as all the photoresist layers. After cleaning each device in oxygen plasma, they are put into a quartz ampoule for inert gas annealing, using a temperature of 250°C.

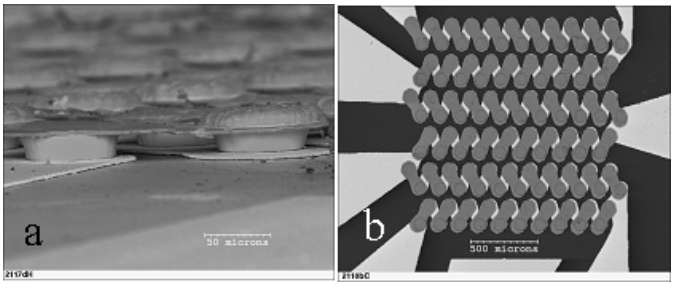

Figure 6. a) SEM close up of a completed p-/n-type couple (~20μm height). b) SEM overview of entire completed mircodevice

Finally, each device must be Cr etched to electrically isolate each bottom gold dogbones and to make certain that each couple is connected electrically in series and not in parallel. The devices are then meticulously cleaned and are allowed to air dry (Figure 6a,b).

Testing and analysis

Two isolated gold triangles within each device (Figure 2a) were used to test for electrical discontinuity, in order to ensure that all the exposed Cr was completely etched away. Typical string resistances range from 2.6Ω to 5 Ω and total device resistances range from 12 to 30Ω (all 6 strings). In fact, string resistances were generally lower after passing current through them. In some cases, as low as 1 ohm per string. Higher resistances were usually attributed to poor or incomplete component contacts and were considered "bad" strings.

In power generation mode, a device was simply mounted on a copper or aluminum block and wired to a computer controlled multimeter and power supply. A 75 watt lamp was illuminated above a glass substrate device, with 4 working strings, as an IV curve was taken and plotted for maximum power. As shown in Figure 7, power generated was about 1 µW. For both glass and silicon substrate devices, about 1mV/string was produced. This translated to a delta T of approximately 1.25K ($V=\alpha_{pn}\Delta T$, seebeck value obtain from cooling mode). The low power can be attributed to a small ΔT and non-optimal materials properties (primarily low Seebeck).

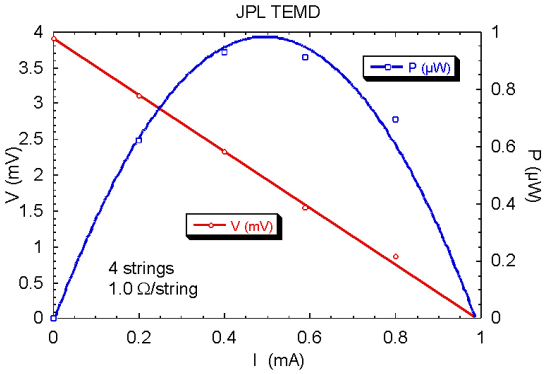

Figure 7. A 75 watt lamp was illuminated above a device, with 4 working strings, as an IV curve was taken and translated into a power curve. As shown, power generated was about 1 µW for this device.

In cooling mode, a device on a Si/SiO_2 substrate was mounted on a temperature controlled heat sink (thick copper disk on commercial thermoelectric stage) and sealed in a vacuum chamber (~10^{-6} torr). A PM390 IR camera with temperature resolution of 0.1°C was setup directly above the device. Thermogram Pro (Thermoteknix) software was used to convert 256 levels of luminosity from the camera into temperature. The software included an image subtraction feature used for determining delta temperature changes from device off/on states. Emissivity corrections for the nickel interconnects were performed at around 70°C, and during testing, hotside temperature was held at 90°C (drifted to 82°C during experiment).

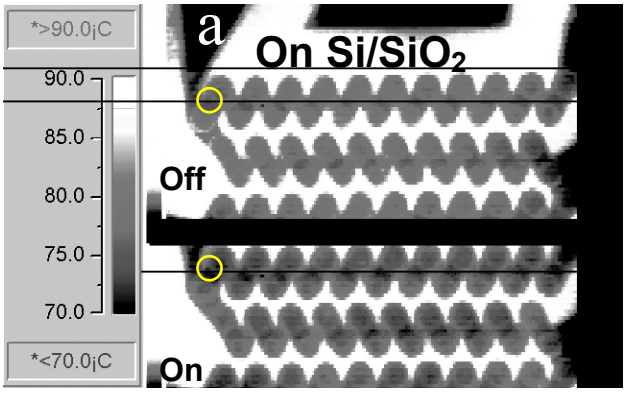

Figure 8a. Split screen thermal images of the same 3 device strings captured by IR camera (color figure translated to black and white). The Si/SiO_2 microdevice was held at 82°C due to low emissivity of nickel. Temperature averaging was performed within circled area. The temperature difference between the off (no current) and on (passing current) states, was determined to be around 2K.

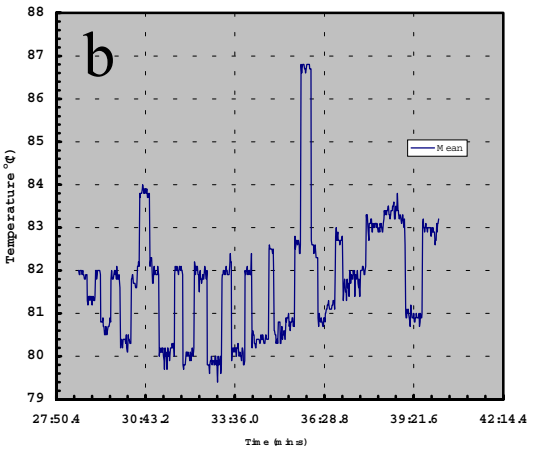

Figure 8b. The Si/SiO_2 microdevice was held at 82°C due to low emissivity of nickel. Temperature averaging was performed within circled area. Notice two intermittent temperature peaks at 84°C and near 87°C. These peaks correspond to negative applied current.

This was done in order to overcome the low emissivity value of nickel and to amplify the heat flux signal. High lustrous materials, such as metals have low emissivity values (E = 0.1 – 0.5). High emissivity (E = 0.7 – 0.9) materials are ceramics or black paint. Temperature was calibrated using high emissivity black carbon tape. A small portion of a top nickel interconnect was sampled and within the sampled area, temperature averaging was evaluated in the "off" and "on" states at various applied currents (Figure 8a.b). Cooling delta vs. applied current was plotted and illustrates a delta max at around 2 K (Figure 9). Calculations indicate that resistivity is indeed low but that effective Seebeck is small. The effective ZT and the effective Seebeck coefficient were calculated using experimental values and equations 1 and 2.

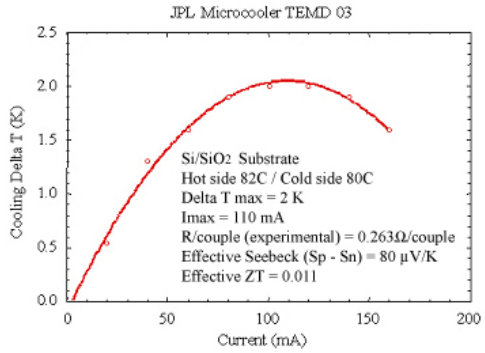

Figure 9. Cooling delta (from temperature averaging) vs. applied current was plotted and illustrates a Delta max at around 2 K.

$$\Delta T_{\max} = \frac{1}{2} Z T_C^2 \qquad [1]$$

Where ΔT_{max} is 2 K from Figure 9, T_c = 353 K (80°C) and Z is the thermoelectric figure of merit. Solving for Z yields 3.2 x 10^{-5} (1/K) and effective ZT = 0.011.

$$I_{\max} = \frac{\alpha_{pn} T_c}{R} \qquad [2]$$

Where I_{max} is 110 mA from Figure 9, T_c = 353 K (80°C), α_{pn} = Seebeck coefficient of p-n couple and R = 0.263Ω/couple. Solving for α_{pn} computes approximately 80 μV/K. The best results were obtained from Si/SiO_2 substrates due to the high thermal conductivity substrate for easier heat dissipation.

Conclusion

At JPL, we have developed a process to fabricate thermoelectric microdevices using a combination of standard integrated circuit techniques and versatile electrochemical deposition methods. Although, a fabrication process has been established, it is obvious that efforts in materials optimization must be pursued. For example, elements with 1mΩcm resistivity were expected to possess a resistance of approximately 0.15Ω/couple and a Seebeck of 160 μV/K (S_n = -60 μV/K and S_p ~100 μV/K). These values are different from those obtained experimentally.

Clearly, there are many materials and miniaturization issues at such small dimensions, one being contact resistance. Increasing aspect ratios will hopefully alleviate contact resistance concerns and enable a greater ΔT. More importantly, the optimization of both ECD thermoelectric materials, n-Bi_2Te_3 and p-$Bi_{2-x}Sb_xTe_3$, must be investigated further in order to attain near bulk transport properties. Specifically improving p-type resistivity, Seebeck and thermal properties. Lastly, other avenues for device evaluation must also be considered. For instance, such as in cooling mode, it is unclear how device performance is effected by operating at elevated temperatures.

Recent work has been focused on increasing device height (aspect ratio), as shown in figure 10. In order to accomplish and accommodate the demands of various applications, in particular in the optoelectronics industry, our thermoelectric microdevices still need to evolve in design, ECD materials properties, and performance.

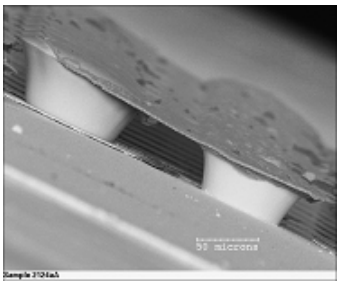

Figure 10. Close up of a p-$Bi_{2-x}Sb_xTe_3$ and n-Bi_2Te_3 couple. The completed microdevice on glass contains elements nearing 40 microns in height.

Acknowledgments

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